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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/644,160

08/20/2003

Wai Wong Chow

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08/19/2004

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EXAMINER

NGUYEN, THINH T

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 08/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/644,160

Applicant(s)

CHOW ET AL.

Examiner

Thinh T Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 and 36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 and 36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED OFFICE ACTION

1. Applicant election for prosecution without traverse of claims 1-15 and 36 is acknowledged.

Specification

2. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b/e) that form the basis for the rejections under this section made in this office action.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1,2 ,4,8,9,14 are rejected under 35 U.S.C. 102(b) as being anticipated by Carter Jr. et al. (U.S. Patent 6, 211,462). or Hisano et al. (US patent 6,376,905)

REGARDING CLAIM 1,2

Carter Jr et al. (fig 2a,fig 2b, the abstract, column 3 lines 39-40) disclose a leadframe for a semiconductor device, the leadframe comprising: a first leadframe portion (fig2a, reference 203) having a perimeter that defines a cavity and a plurality of leads extending inwardly from the perimeter, wherein the first leadframe portion has a first thickness; and a second leadframe portion attached to the first leadframe portion, the second leadframe portion having a die paddle received within the cavity of the first leadframe portion, wherein the second leadframe portion (fig 21a reference 201) has a second thickness that is greater than the first thickness.

Similarly, Hisano et al. (the abstract, fig 2, portion 3 and 6, fig 6 portion 13 and 6) disclose the same invention.

REGARDING CLAIM 4

Carter Jr et al. (Column 6 line 10) disclose a leadframe made of metal and similarly, Hisano et al. (the abstract, fig 2,fig 6) disclose the same invention.

REGARDING CLAIM 8

Carter Jr et al. (fig 2a,fig 2b, the abstract, column 3 lines 39-40) disclose a semiconductor device, comprising: a first leadframe portion having a plurality of leads that surround a cavity, wherein the first leadframe portion has a first thickness; a second leadframe portion attached the first leadframe portion, the second leadframe portion having a die paddle received within the cavity of the first leadframe portion, wherein the second leadframe portion has a second thickness; an integrated circuit die attached to the die paddle, located within the cavity and

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surrounded by the plurality of leads, the die including a plurality of die pads; and a plurality of wires electrically connecting respective ones of the die pads with corresponding ones of the leads.

Similarly, Hisano et al. (the abstract, fig 2, fig 6) disclose the same invention.

REGARDING CLAIM 9

Carter Jr et al. (fig 2a, fig 2b, the abstract, column 3 lines 39-40) disclose a semiconductor device comprising an encapsulant covering a top surface of the integrated circuit die, the wires, and the a top surface the leads, wherein at least a bottom surface of the leads and a bottom surface of the second leadframe portion are exposed.

Similarly, Hisano et al. (the abstract, fig 2, fig 6) disclose the same invention.

REGARDING CLAIM 14

Carter Jr et al. (fig 2a, fig 2b, the abstract, column 3 lines 39-40) disclose a semiconductor device comprising: a first metal leadframe portion having a plurality of leads surrounding a cavity, wherein the first leadframe portion has a first thickness; a second metal leadframe portion attached to the first leadframe portion and electrically isolated therefrom, the second leadframe portion having a die paddle received within the cavity, wherein the second leadframe portion has a second thickness that is greater than the first thickness; an integrated circuit die attached to the die paddle, located within the cavity and surrounded by the plurality of leads, the die including a plurality of die pads; a plurality of wires electrically connecting respective ones of the die pads with corresponding ones of the leads; and an encapsulant covering a top surface of the integrated circuit die, the wires, and a top surface of the leads, wherein at least a bottom surface of the leads and the second leadframe are exposed.

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Similarly, Hisano et al. (the abstract, fig 2, fig 6) disclose the same invention.

5. Claim 36 is rejected under 35 U.S.C. 102(e) as being anticipated by Crowley et al. (US patent 6,396,130).

REGARDING CLAIM 36

Crowley et al. (fig 1, fig 4, fig 5, the abstract, column 4 lines 14-29) disclose a semiconductor device, comprising: a first metal leadframe portion having a plurality of leads surrounding a cavity, wherein the first leadframe portion has a first thickness; a second metal leadframe portion attached to the first leadframe portion and electrically isolated therefrom, the second leadframe portion having a pair of adjacent die paddles received within the cavity, wherein the second leadframe portion has a second thickness that is greater than the first thickness; first and second integrated circuit die attached to respective ones of the die paddles, located within the cavity and surrounded by the plurality of leads, the first and second die each including a plurality of die pads; a plurality of wires electrically connecting respective ones of the die pads of the first and second die with corresponding ones of the leads; and an encapsulant covering a top surface of the first and second integrated circuit die, the wires, and a top surface of the leads, wherein at least a bottom surface of the leads and the second leadframe are exposed.

6. Claim 5, 6, 10, 11, 13, 15 are rejected under 35 U.S.C. 102 (b) as being anticipated by Hisano et al. (US Patent 6,376,905)

REGARDING CLAIM 5, 6, 13, 15

Hisano et al. (the abstract, fig 2, fig 6) disclose a leadframe for a semiconductor device

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wherein first and second leadframe portions are formed of copper and wherein the first and second leadframe portions are electrically isolated from each other.

REGARDING CLAIM 10,11

Hisano et al. (the abstract, fig 2, fig 6) disclose a leadframe for a semiconductor device wherein the first and second leadframe portions are formed of copper and wherein the second thickness is greater than the first thickness.

Claim Rejections - 35 USC § 103

7. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 3,7,12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hisano et al. (US patent 6,376,905) in view of further remark.

REGARDING CLAIM 3,7,12

Hisano et al.(the abstract, fig 2, fig 6) disclose all the invention except for the specific thickness or relative thickness of the leadframe portions.

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These features are considered obvious since a person skilled in the art at the time the invention was made would have been motivated to find the optimum value using his routine design skill and the teachings by Hisano et al in order to come up with the invention of claims 3,7,12 for a purpose of optimizing and improving the semiconductor device.

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

11. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

CONCLUSION

12. The prior arts made of record and not relied upon are considered pertinent to applicant disclosure: Takiar (US patent 5,625,235) disclose a multichip integrated module with crossed bonding wires.

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13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790.

The examiner can normally be reached on Monday-Friday 9:00am-6:00pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached at 571-272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thinh T. Nguyen TTN

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David Nelms
Supervisory Patent Examiner
Technology Center 2800